EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S3	26	(integrated adj circuit) same (reset adj control adj signal)	USPAT	OR	OFF	2006/12/14 08:30
S4	0	(first adj integrated adj circuit) same (reset adj control adj signal)	USPAT	OR	OFF	2006/12/14 08:30
S5	0	(two adj integrated adj circuit) same (reset adj control adj signal)	USPAT	OR	OFF	2006/12/14 08:30
S6	1	(two adj integrated adj circuit) and (reset adj control adj signal)	USPAT	OR	OFF	2006/12/14 08:33
S7	0	(inter adj integrated adj circuit) and (reset adj control adj signal)	USPAT	OR	OFF	2006/12/14 08:34
S8	4	(plurality adj integrated adj circuit) and (reset adj control adj signal)	USPAT	OR	OFF	2006/12/14 09:04
S9	17	("20020046377" | "20020174394" | "20030016578" | "4333142" | "5222066" | "5388104" | "5475815" | "5535164" | "5617531" | "5835502" | "5974579" | "5995731" | "6085346" | "6163490" | "6209074" | "6360342" | "6446184").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2006/12/14 08:35
S10	1823	(integrated adj circuit) and (reset near control)	USPAT	OR	OFF	2006/12/14 08:36
S11	1500	(integrated adj circuit) and (reset adj control)	USPAT	OR	OFF	2006/12/14 08:36
S12	144	"327"/$.ccls. and (integrated adj circuit) and (reset adj control)	USPAT	OR	OFF	2006/12/14 08:58
S13	85	"327"/$.ccls. and (driver) and (reset adj control)	USPAT	OR	OFF	2006/12/14 09:02
S14	0	"327"/$.ccls. and (integrate adj circuit adj domain) and (reset adj control)	USPAT	OR	OFF	2006/12/14 08:39
S15	1	"327"/$.ccls. and (integrate adj circuit) and (reset adj control)	USPAT	OR	OFF	2006/12/14 08:39
S16	12	"327"/$.ccls. and (driver and receiver) and (reset adj control)	USPAT	OR	OFF	2006/12/14 08:39
S17	1	"6292116".pn.	USPAT	OR	OFF	2006/12/14 08:43
S18	1	"6199135".pn.	USPAT	OR	OFF	2006/12/14 08:43
S19	7	"327"/$.ccls. and (integrated adj circuit) and (generat$6 near (reset adj control))	USPAT	OR	OFF	2006/12/14 08:59
S20	1	"375"/$.ccls. and (integrated adj circuit) and (generat$6 near (reset adj control))	USPAT	OR	OFF	2006/12/14 09:00

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S21	0	"327"/$.ccls. and (driver) and receiver and (generat$6 near (reset adj control))	USPAT	OR	OFF	2006/12/14 09:03
S22	10	(driver) and receiver and (generat$6 near (reset adj control))	USPAT	OR	OFF	2006/12/14 09:03
S23	12	(clock adj domain) and (reset adj control adj signal)	USPAT	OR	OFF	2006/12/14 09:06
S24	0	(clock adj domain) and (generat$8 near (reset adj control adj signal))	USPAT	OR	OFF	2006/12/14 09:07
S25	60	(clock) and (generat$8 near (reset adj control adj signal))	USPAT	OR	OFF	2006/12/14 09:11
S26	3	"710"/$.ccls. and (clock) and (generat$8 near (reset adj control adj signal))	USPAT	OR	OFF	2006/12/14 09:12
S27	11	"327"/$.ccls. and (clock) and (generat$8 near (reset adj control adj signal))	USPAT	OR	OFF	2006/12/14 09:14
S28	0	"327"/$.ccls. and (drviver and receiver and clock)	USPAT	OR	OFF	2006/12/14 09:14
S29	841	"327"/$.ccls. and (driver and receiver and clock)	USPAT	OR	OFF	2006/12/14 09:14
S30	222	"327"/$.ccls. and (driver same receiver same clock)	USPAT	OR	OFF	2006/12/14 09:16
S31	2	"327"/$.ccls. and (driver same receiver same clock same (reset adj signal))	USPAT	OR	OFF	2006/12/14 09:17
S32	147	"327"/$.ccls. and (driver same (reset adj signal))	USPAT	OR	OFF	2006/12/14 10:57
S33	5	(driver near generat$6 near (reset adj signal))	USPAT	OR	OFF	2006/12/14 13:27
S34	1	"5479448".pn.	USPAT	OR	OFF	2006/12/14 13:40
S35	0	inter near2 (reset adj control adj signal)	USPAT	OR	OFF	2006/12/14 16:01
S36	0	inter with (reset adj control adj signal)	USPAT	OR	OFF	2006/12/14 16:01
S37	10	driver with (reset adj control adj signal)	USPAT	OR	OFF	2006/12/14 16:07
S38	3	driver with generat$8 with (reset adj control adj signal)	USPAT	OR	OFF	2006/12/14 16:06
S39	0	(reset adj control adj signal) same (integrated adj circuit adj domain)	USPAT	OR	OFF	2006/12/14 16:31
S40	26	(reset adj control adj signal) same (integrated adj circuit)	USPAT	OR	OFF	2006/12/14 17:42
S41	2	"455"/$.ccls. and (ADC with (low adj power))	USPAT	OR	OFF	2006/12/14 17:44

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S42	4	"455"/$.ccls. and (ADC with (power near sav$8))	USPAT	OR	OFF	2006/12/14 17:45
S43	0	"455"/$.ccls. and (ADC same (power near conserva$8))	USPAT	OR	OFF	2006/12/14 17:45
S44	0	"455"/$.ccls. and (ADC same (power near saving$8) same preamble)	USPAT	OR	OFF	2006/12/14 17:46
S45	0	"455"/$.ccls. and (preamble same (separate adj path))	USPAT	OR	OFF	2006/12/14 17:46
S46	0	"455"/$.ccls. and (preamble and (separate adj path))	USPAT	OR	OFF	2006/12/14 17:46
S47	119	"455"/$.ccls. and (preamble and (power adj sav$8))	USPAT	OR	OFF	2006/12/14 17:47
S48	20	"455"/$.ccls. and (preamble same (power adj sav$8))	USPAT	OR	OFF	2006/12/14 17:48
S49	0	"455"/$.ccls. and ((dual near ADC) same (power adj sav$8))	USPAT	OR	OFF	2006/12/14 17:53
S50	1	"6650624".pn.	USPAT	OR	OFF	2006/12/14 17:53
S51	69	modem with (reset adj signal)	USPAT	OR	OFF	2006/12/15 07:55
S52	227460	orthogonal adj variable addj spread	USPAT	OR	OFF	2006/12/15 07:55
S53	3	orthogonal adj variable adj spread	USPAT	OR	OFF	2006/12/21 15:04
S54	0	10/094848	USPAT	OR	OFF	2006/12/15 10:13
S55	0	"10094848"	USPAT	OR	OFF	2006/12/15 14:46
S56	0	10/621056	USPAT	OR	OFF	2006/12/15 14:46
S57	0	"10621056"	USPAT	OR	OFF	2006/12/15 14:47
S58	0	"20040013209"	USPAT	OR	OFF	2006/12/15 14:47
S59	1	"2004/0013209"	USPAT	OR	OFF	2006/12/15 14:47
S60	1	"6839570"	USPAT	OR	OFF	2006/12/21 15:03
S61	1	"6690719".pn.	USPAT	OR	OFF	2006/12/21 15:03
S62	11	375/222.ccls. and (internal adj reset)	USPAT	OR	OFF	2006/12/21 15:05

Day : Thursday
Date: 12/21/2006

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Time: 16:21:27

Inventor Name Search Result

Your Search was:

Last Name = RADJASSAMY
First Name = RAJAKRISHNAN

Application#	Patent#	Status	Date Filed	Title	Inventor Name
09617373	6310499	150	07/17/2000	Methods and apparatus for adjusting the deadtime between non-overlapping clock signals	RADJASSAMY, RAJAKRISHNAN
09620932	6331800	150	07/21/2000	Post-silicon methods for adjusting the rise/fall times of clock edges	RADJASSAMY, RAJAKRISHNAN
09938206	6931562	150	08/23/2001	SYSTEM AND METHOD FOR TRANSFERRING DATA FROM A HIGHER FREQUENCY CLOCK DOMAIN TO A LOWER FREQUENCY CLOCK DOMAIN	RADJASSAMY, RAJAKRISHNAN
09938210	6928574	150	08/23/2001	SYSTEM AND METHOD FOR TRANSFERRING DATA FROM A LOWER FREQUENCY CLOCK DOMAIN TO A HIGHER FREQUENCY CLOCK DOMAIN	RADJASSAMY, RAJAKRISHNAN
10005758	6407602	150	11/02/2001	POST-SILICON METHODS FOR ADJUSTING THE RISE/FALL TIMES OF CLOCK EDGES	RADJASSAMY, RAJAKRISHNAN
10376390	Not Issued	30	02/28/2003	Register-based de-skew system and method for a source synchronous receiver	RADJASSAMY, RAJAKRISHNAN
10376835	Not Issued	71	02/28/2003	System and method for establishing a known timing relationship between two clock signals	RADJASSAMY, RAJAKRISHNAN
10393192	Not Issued	161	03/20/2003	System and method for estimating power consumption for at least a portion of an	RADJASSAMY, RAJAKRISHNAN

				integrated circuit	
10622672	Not Issued	30	07/18/2003	Reset scheme for I/O pads in a source synchronous system	RADJASSAMY, RAJAKRISHNAN
11085693	Not Issued	41	03/21/2005	Double-high Dimm with Dual Registers and Related Methods	RADJASSAMY, RAJAKRISHNAN
60469500	Not Issued	159	05/10/2003	Reset scheme in a synchronous system	RADJASSAMY, RAJAKRISHNAN

Inventor Search Completed: No Records to Display.

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